REMARKS

Applicants appreciate the examination of the application that is evidenced by the Official Action of November 7, 2005. Applicants also appreciate the indication that Claims 4-5, 25-26 and 44-45 recite allowable subject matter. Applicants also submit that Claims 6-8, 27-29 and 46 must also recite allowable subject matter because Claims 6-8 depend directly or indirectly from Claim 4, Claims 27-29 depend directly or indirectly from Claim 25 and Claim 46 depends directly from Claim 44.

In response to the Official Action, Applicants have rewritten Claims 4, 25 and 44 in independent form and Claims 40-41 have been canceled. Thus, the sole outstanding issue is the patentability of Claims 1-3, 9-24, 30-39 and 42-43 in view of the cited prior art.

Claims 1-3, 9-24, 30-39 and 42-43 are Patentable over the Cited Prior Art

Independent Claims 1, 16, 24, 37 and 42 have been amended to highlight additional features of the present invention. In the embodiment of the invention illustrated by FIG. 2, the result status registers **80** store a plurality of result status (RS) signals, which are provided to an interrupt indication circuit **60a** and a non-interrupt indication circuit **60b**. In addition, result status select registers **70** store a plurality of result status select (RSS) signals. These result status select (RSS) signals are also provided to the interrupt indication circuit **60a** and the non-interrupt indication circuit **60b**. As described throughout the application, the multi-bit value of the RSS signal <0:127> determines whether a corresponding RS signal <0:127> is processed by the interrupt indication circuit **60** or the non-interrupt indication circuit **60b**. In particular, the RSS signal <0:127> is provided to the first and second banks **62a** and **62b**. In this manner, the AND gates in the first and second banks **62a** and **62b** control which ones of the individual RS signals pass to the OR gate **68a** and which ones pass to the OR gate **68b**.

To reflect these features of the embodiment illustrated by FIG. 2, Claim 1 has been amended to recite that the control circuit, which is highlighted at page 6 of

the application, is further configured to "generate a plurality of result status select signals (e.g., RSS<0:127>) that indicate whether or not corresponding ones of the plurality of result status signals (e.g., RS<0:127>) are to be used by said control circuit to generate an aggregate result status signal (e.g., ARS) as the at least one signal". For example, if RSS<0:127> equals <111100000...all zeros...0001010>, then RS<0>, RS<1>, RS<2>, RS<3>, RS<124> and RS<126> will be processed by the interrupt indication circuit **60a** and RS<4>, RS<5>, ..., RS<122>, RS<123>, RS<125> and RS<127> will be processed by the non-interrupt indication circuit **60b** in order to generate the aggregate result status signal (ARS). Applicants respectfully submit that none of the cited prior art references, even when combined, disclose or suggest these aspects of Claim 1.

Similar arguments also apply to amended independent Claims 16, 24, 37 and 42. For example, Claim 16 has been amended to recite that the control circuit is further configured to "generate a plurality of result status select signals (e.g., RSS<0:127>) that indicate whether or not corresponding ones of the plurality of result status signals (e.g., RS<0:127>) are to be used by said control circuit to generate the at least one interrupt". As described in the application, the at least one interrupt is generated by the interrupt indication circuit **60a**.

Based on these arguments, Applicants respectfully submit that all pending claims are in condition for allowance, which is respectfully requested.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on November 28, 2005.

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